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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Chambers et al.

Art Unit: 2818

Serial No.: 10/696,539

Examiner: Tran, M.

Filing Date: 10/29/2003

Docket No.: TI-36031

Customer No.: 23494

Conf. No.: 7816

Title: TRIPLE-GATE MOSFET TRANSISTOR AND METHODS FOR
FABRICATING THE SAME

ELECTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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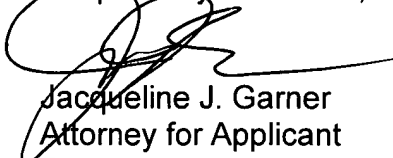
Date

Marianna Smith

Dear Sir:

With respect to the Restriction Requirement mailed on 09/27/2004, the Examiner has restricted the instant application to the invention of Group I (Claims 11-24), or Group II (Claims 1-10). In light of this, Applicants elect to pursue Group II, (Claims 1-10) without traverse.

Respectfully submitted,


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